

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,829,183 B2
DATED : December 7, 2004
INVENTOR(S) : George M. Braceras

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Delete the title page and substitute therefore the attached title page.

Delete Drawing Sheets 1-9 and substitute therefore the attached Drawing Sheets 1-9.

Signed and Sealed this

Thirty-first Day of May, 2005



JON W. DUDAS
Director of the United States Patent and Trademark Office

(12) United States Patent
Braceras(10) Patent No.: US 6,829,183 B2
(45) Date of Patent: Dec. 7, 2004

(54) ACTIVE RESTORE WEAK WRITE TEST MODE

(58) Field of Search 365/201, 200,
365/230.06, 185.09, 185.2, 210(75) Inventor: George M. Braceras, Essex Junction,
VT (US)

(56) References Cited

(73) Assignee: International Business Machines
Corporation, Armonk, NY (US)

U.S. PATENT DOCUMENTS

(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.

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(21) Appl. No.: 10/665,254

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(22) Filed: Sep. 20, 2003

Primary Examiner—Connie C. Yoha
(74) Attorney, Agent, or Firm—Robert A. Walsh

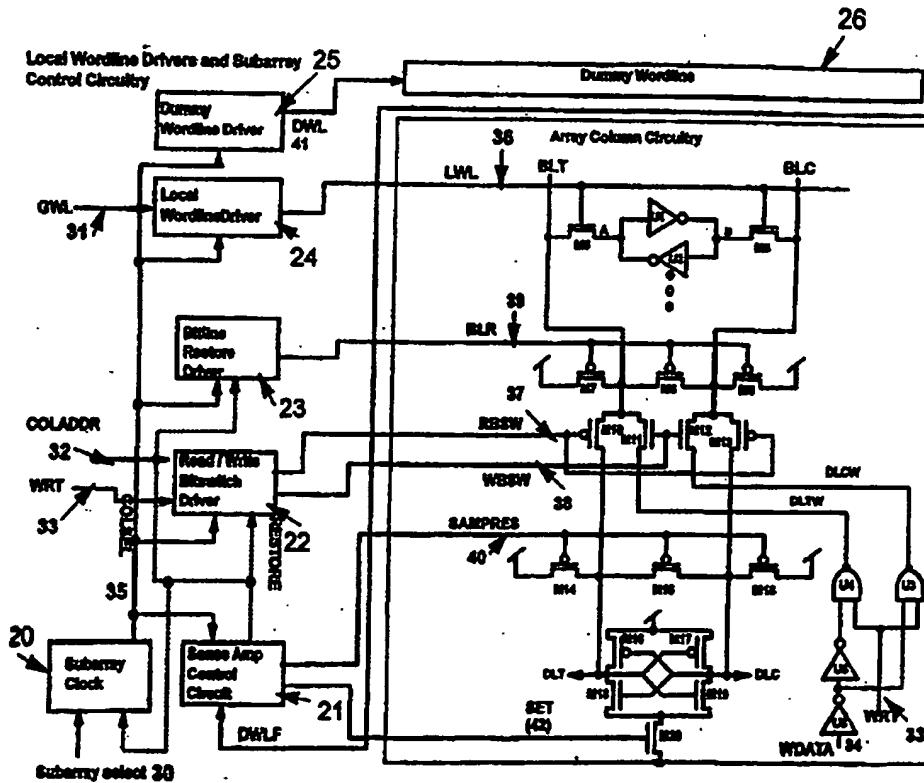
(65) Prior Publication Data

(57) ABSTRACT

US 2004/0062105 A1 Apr. 1, 2004

A semiconductor memory device having an active restore weak write test mode for resistive bitline contacts. During the write margin test a circuit is used to block the bitline restore devices from turning off during the SRAM write cycle.

4 Claims, 9 Drawing Sheets

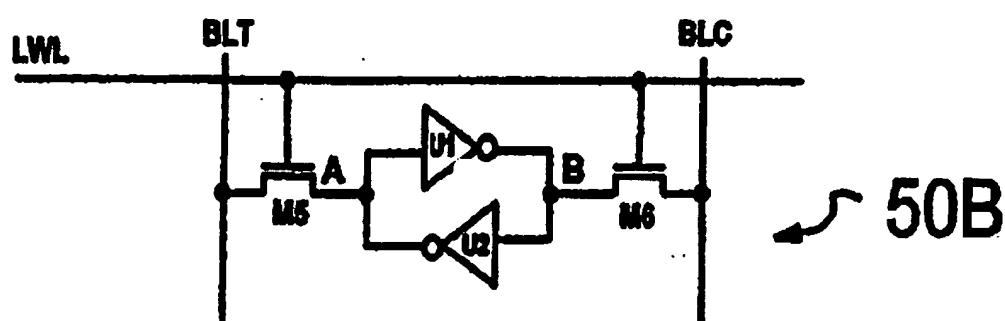
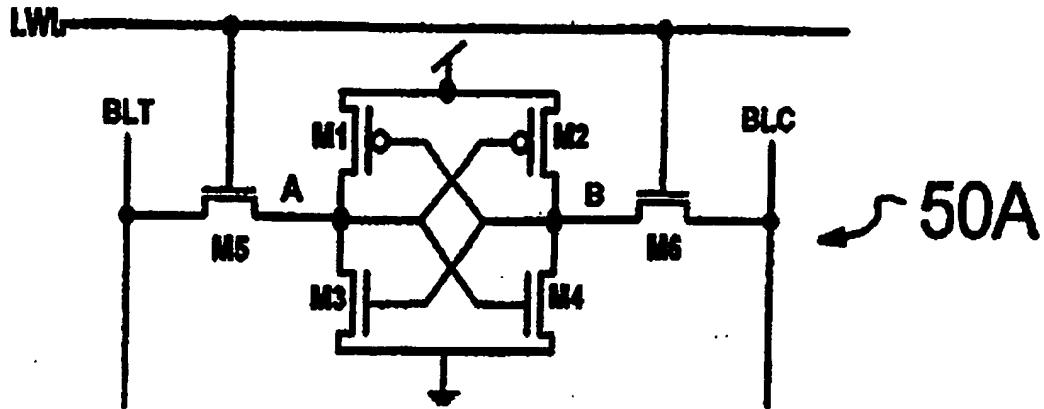


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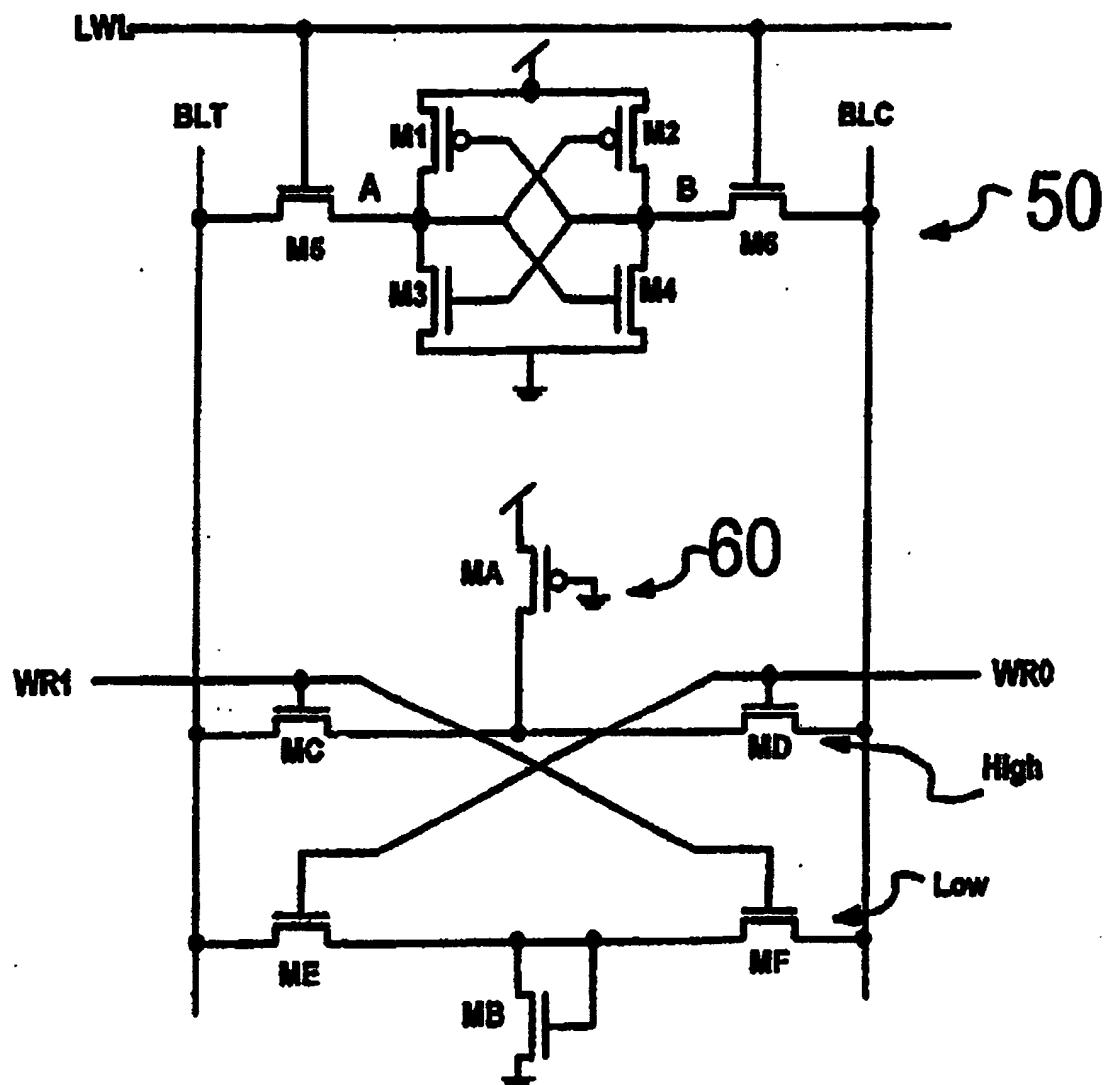
(Prior Art)
FIG. 1A

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(Prior Art)
FIG. 1B

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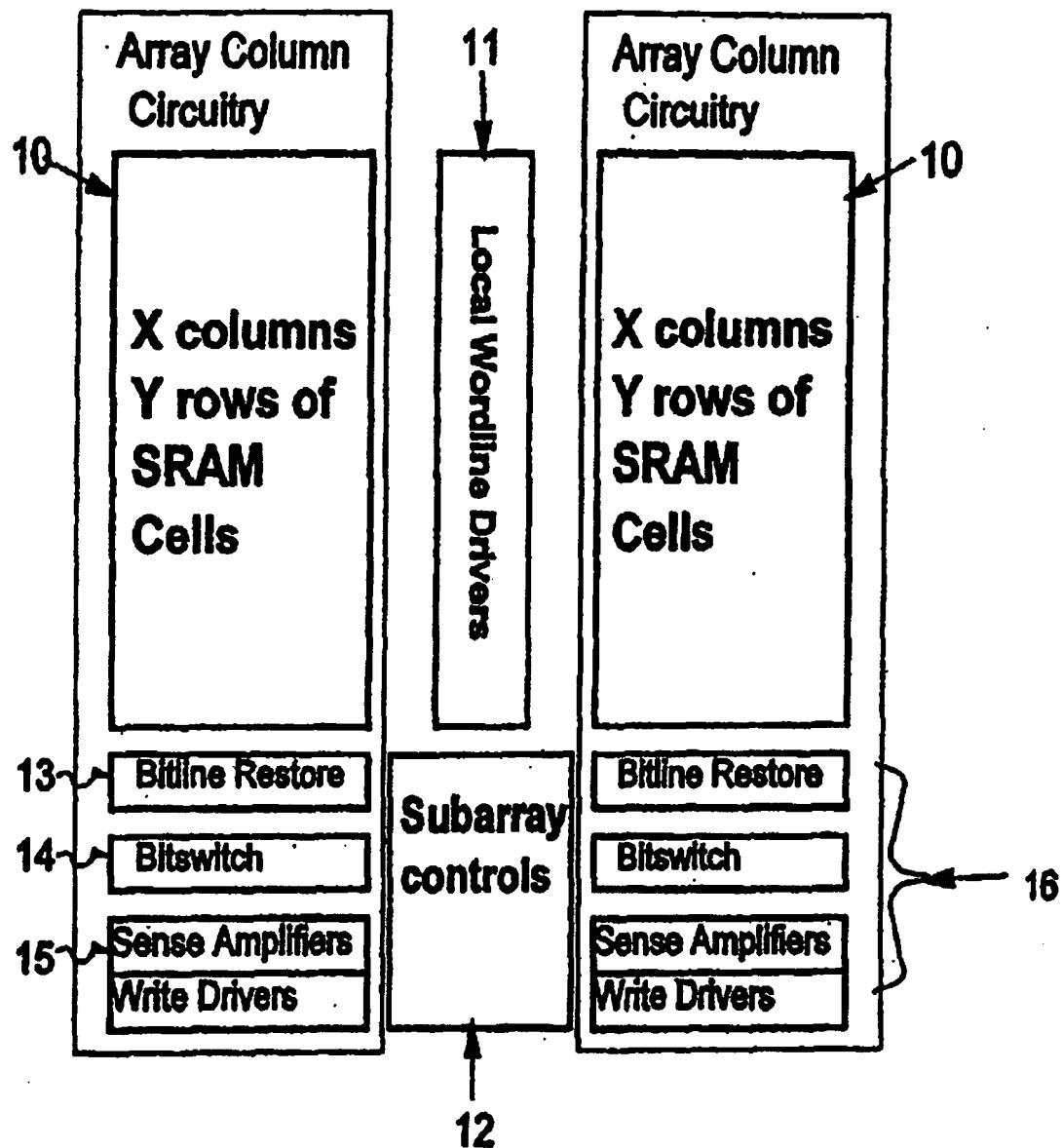


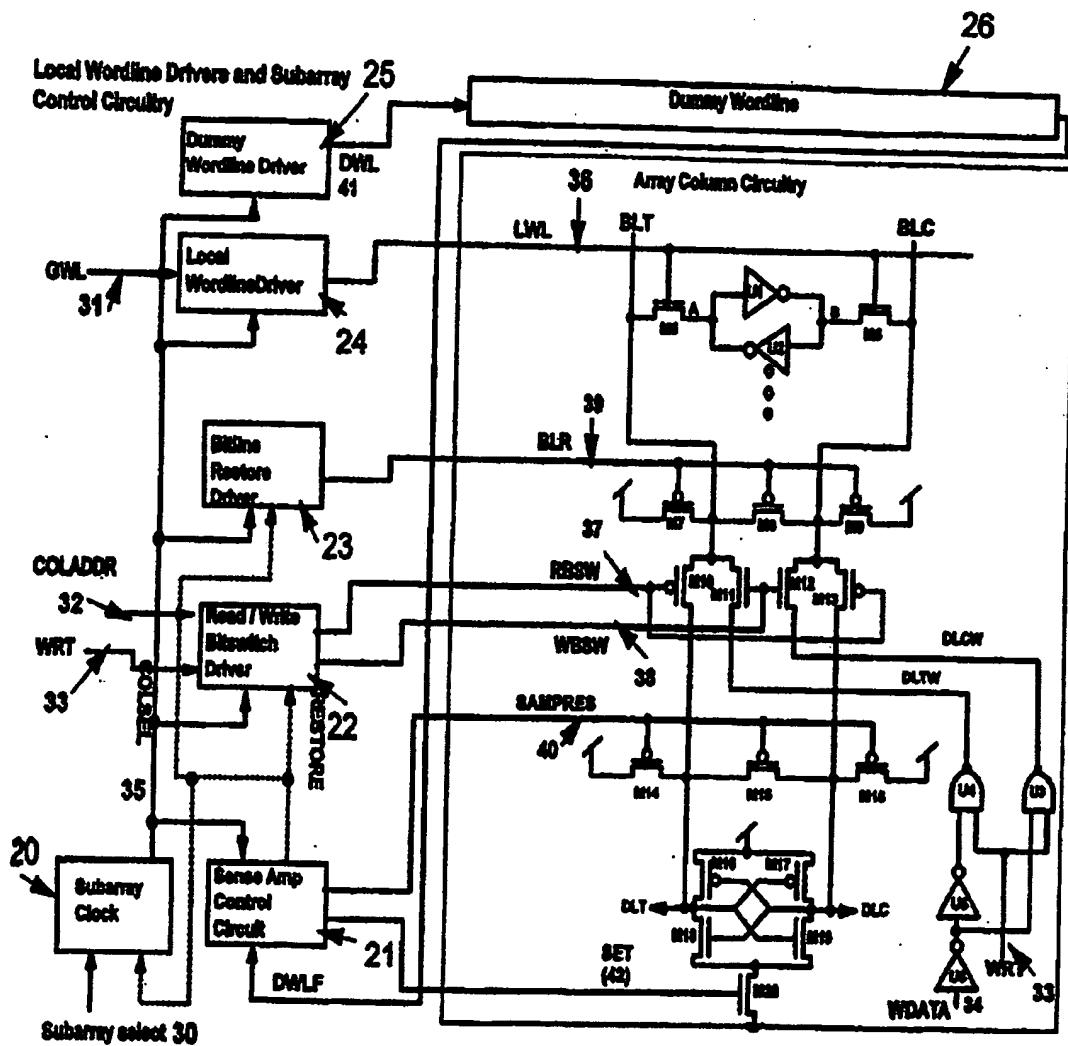
Fig. 2

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(Prior Art)

FIG. 3

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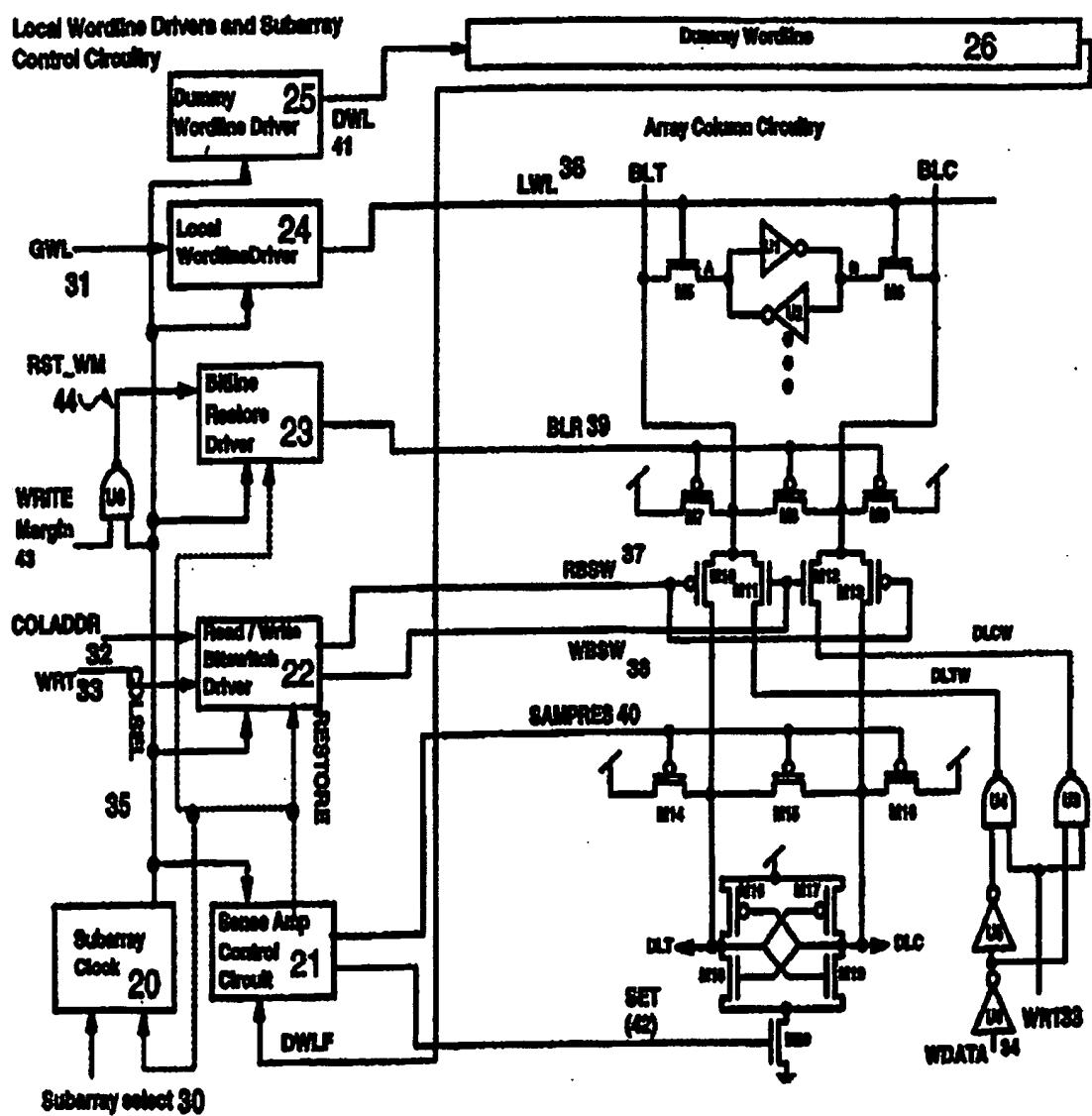


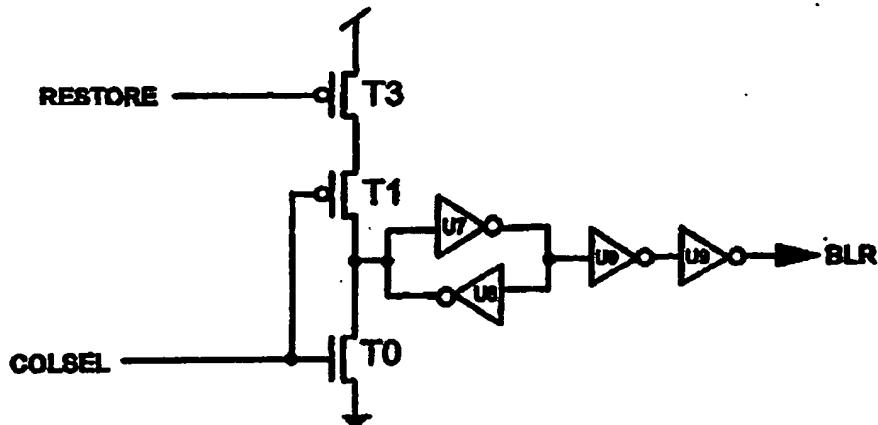
FIG 4

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(Prior Art)
FIG 5A

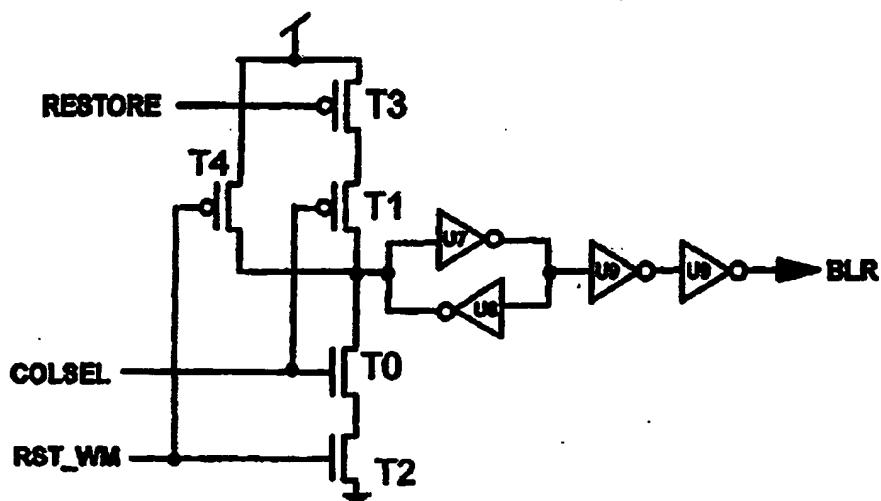


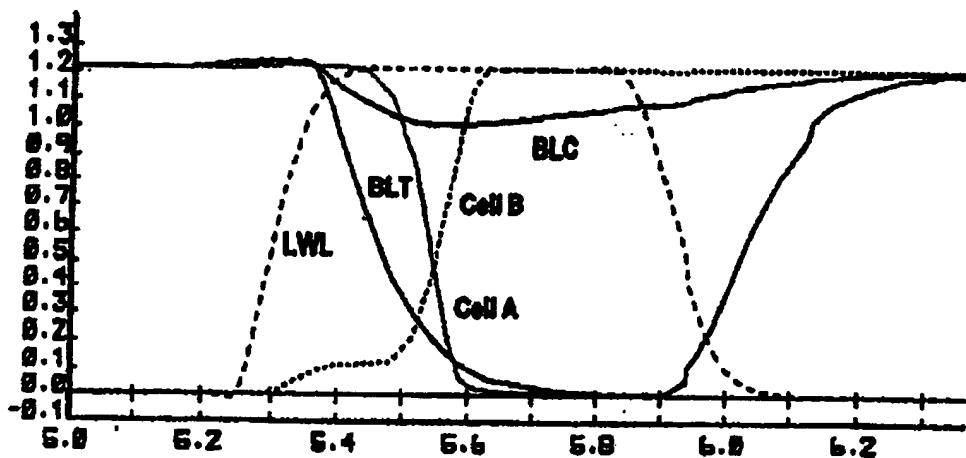
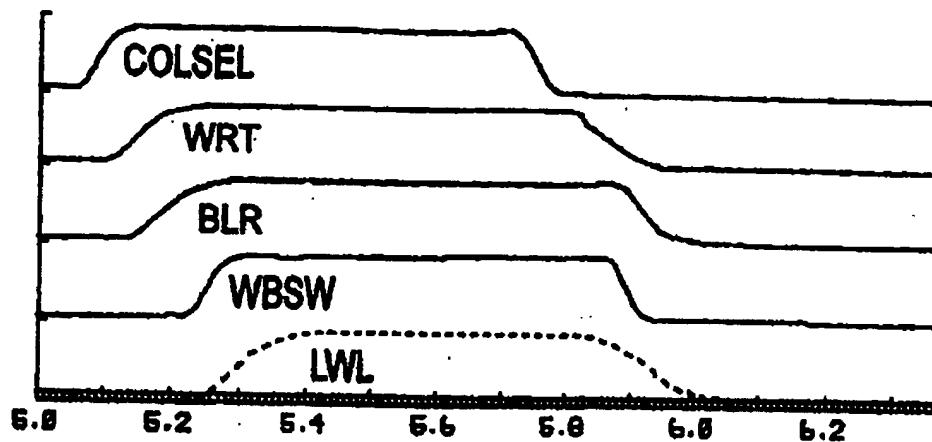
FIG 5B

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(Prior Art)

FIG 6A

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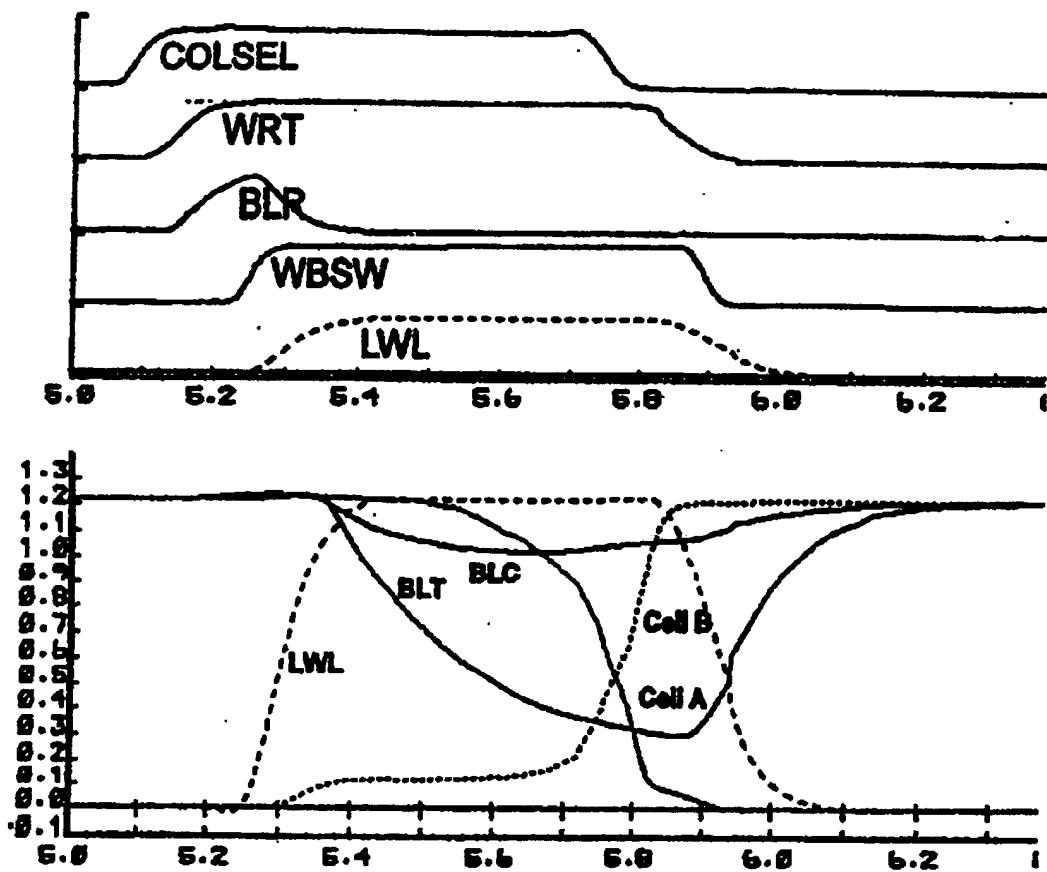


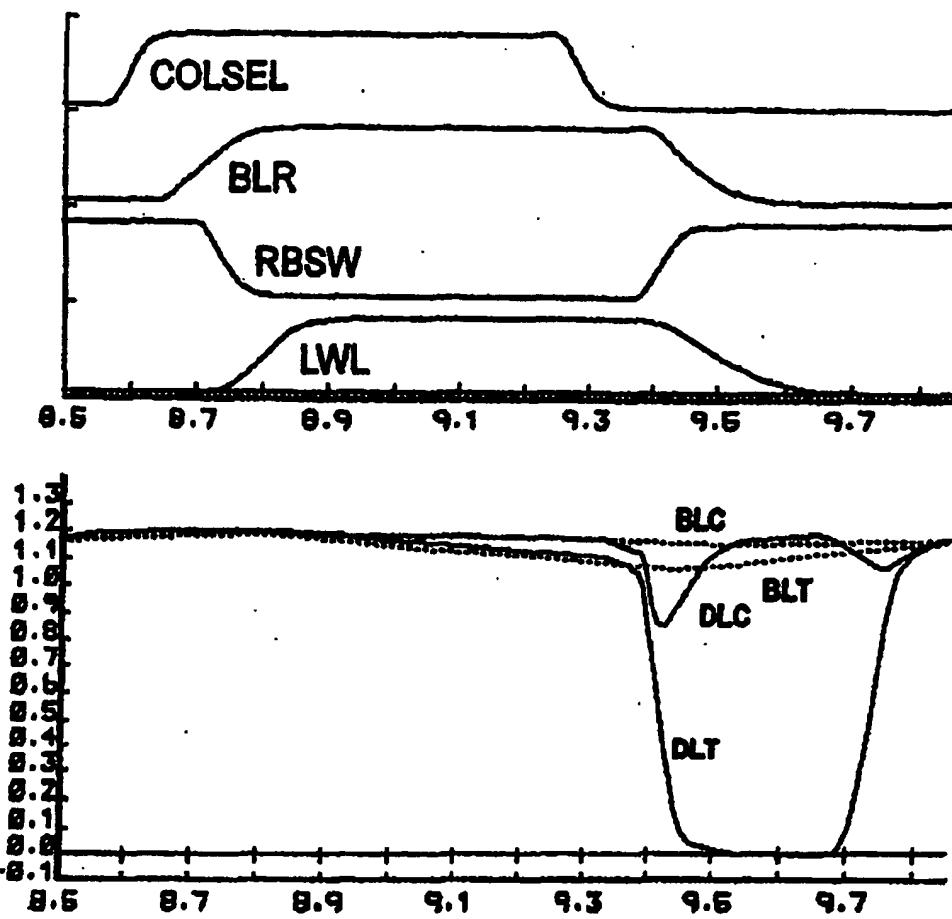
FIG 6B

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(Prior Art)

FIG. 6C